M.Tech in VLSI Design

SEMESTER I

DIGITAL VLSI DESIGN:
Introduction to MOSFETs: Fabrication and Modeling (Designer's View-point), MOS Inverter: Static and Switching Characteristics; MOS Capacitor; Resistivity of Various Layers, Symbolic and Physical Layout Systems -- MOS Layers Stick/Layout Diagrams; Issues of Scaling, Combinational MOS Logic Circuits: Pass Transistors/Transmission Gates; Primitive Logic Gates; Complex Logic Circuits, Sequential MOS Logic Circuits: Latches and Flip-flops, Dynamic Logic Circuits; Clocking Issues, CMOS Subsystem Design; Case Studies.

VLSI COMMUNICATION CIRCUITS:
Introduction to basic topics in digital communications and basic RF receiver design using VLSI circuits.,Digital Modulation & Coding techniques, Multi carrier Modulation, Synchronization, Multiplexing, Rake Receiver, CDMA Structure, Super heterodyne receiver, Low noise amplifier, mixers, Analog to Digital converter, Delta Sigma Converter, Phase locked loops, frequency synthesizer and timing recovery circuits.

DSP SYSTEMS & ARCHITECTURE:
Overview of DSP systems fundamentals, DFT,FFT,DCT Structure, Finite word length effect, fixed point and floating point representation, Filter Design and Structures for FIR Filters and IIR Filters, Adpative Filters: FIR adaptive filters-Newton's steepest descent method - adaptive filter based on steepest descent method-Widrow Hoff LMS adaptive algorithm-Adaptive channel equalization-Adaptive echo chancellor-Adaptive noise cancellation-RLS adaptive filters-Exponentially weighted RLS-sliding window RLS-Simplified IIR LMS adaptive filter, Multirate dsp systems: Mathematical description of change of sampling rate - Interpolation and Decimation - continuous time model - Direct digital domain approach - Decimation by an integer factor - Interpolation by an integer factor - Single and multistage realization –CIC Filter- poly phase realization - Application to sub band coding - Wavelet transform and filter bank implementation of wavelet expansion of signals, Programmable DSP architecture: Memory structure and Addressing, Pipelining, VLIW architecture, Superscalar processor, RISC, CISC

SEMICONDUCTOR DEVICES PHYSICS AND MODELING
Basic Semiconductor Physics; Energy Bands and Charge Carriers; MOS Capacitor. MOSFET and Compound Semiconductor FET and modeling, Schottky Barriers and Ohmic Contacts, Bipolar Junction Transistors and modeling, Recent Developments in Microelectronic Devices.

HDL-BASED DESIGN WITH PROGRAMMABLE LOGIC: VHDL for Behavioural, RTL, Data-flow and Structural Modeling, Verilog for Behavioural, RTL, Data-flow and Structural Modeling, FPGA Architectures and Technology, VHDL Synthesis for FPGA Implementation, Verilog Synthesis for FPGA Implementation.

COMMUNICATION AND DSP LAB :
The laboratory work, assignments, design problem/case study are based on theory DSP Projects : IP core development, e.g.FIR filter using various methods,FFT Structures, Cordic Algorithms implementation, DCT structureCommunication projects: IP core development(System Design),Use of tools such as Xilinx's System Generator, ALTERA DSP builder and MATLAB,Simulink and FPGA development boards, HDL system level simulation and Synthesis Tools.

HDL BASED DESIGN AND SIMULATION LAB:
The laboratory work consists of exercise/ assignments based on designing of adders, subtractors, multiplexers, ALU, memory and other digital circuits. The exercise involves designing of circuits, writing of VHDL codes and implementation on FPGA/CPLD boards. HDL Simulation and Synthesis tools are to be used: e.g.FPGA Advantage from Mentor Graphics, Xilinx Foundation Series, Altera Tools, Development boards of FPGA/ CPLD (Programmable Logic)

SEMESTER II

APPLIED ALGORITHMS FOR VLSI CAD
Review of Graph and Network Flow Algorithms, Dependency/ Constraint graphs; Steiner Tree; Cliques, Clustering and Spanning Tree Algorithms; Integer Programming algorithms, Review of Greedy, Heuristic, Constructive and Iterative Algorithms,Combinatorial Optimization/ Minimization Algorithms, Simulated Annealing, Genetic algorithms Simulated Evolution Algorithms,Scheduling and Allocation algorithms, Partitioning algorithms,Placement Algorithms: Routing algorithms

VLSI SIGNAL PROCESSING:
Introduction to DSP systems - Iteration Bound - Pipelined and parallel processing., Retiming – folding-Unfolding - Algorithmic strength reduction in filters and transforms, Systolic architecture design - fast convolution - Pipelined and parallel recursive and adaptive filters, Scaling and round off noise - Digital lattice filter structures - Bit level arithmetic architecture – Redundant arithmetic, Numerical strength reduction - Synchronous, wave and asynchronous pipe lines - low power design, Programmable digital signal processors.

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IC FABRICATION TECHNOLOGY:
Material properties; Crystal growth; Doping; Diffusion; Oxidation; Epitaxy; Ion Implantation,Deposition of films using CVD, LPCVD and Sputtering Techniques,Wet and Dry Etching and Cleaning; Lithographic Process; Device and Circuit Fabrication, Process Modeling and Simulation.

MIXED SIGNAL VLSI DESIGN :
Current and Voltage Sources; Differential and Operational Amplifiers, Comparators; Voltage References,Passive and Active Parameter Sensitivity and Component Ratioing,Analog Filters (Continuous-Time and Switched-Capacitor); Digital Filters,Sample-and-Hold Circuits,Analog-to-DigitalConverters; Digital-to-Analog Converters, Sigma-Delta Converters.

TESTING AND VERIFICATION OF VLSI DESIGN : Introduction to Testing Concepts; Testing Combinatorial Circuits; Testing Sequential Circuits,Random Pattern Testing, Memory Testing; Analog and Mixed Signal Testing; Delay Testing; IDDQ Testing, DFT Techniques; BIST Techniques, Boundary Scan Architecture and Testing, Functional and Formal Verification
SoC and Embedded System Testing; Future Trends.

ANALOG IC DESIGN LAB :
VLSI Design: Familiarization with EDA tools for schematic and layout entry, circuit simulation using SPICE,DC transfer Characteristics of Inverters, Transient response, Calculating propagation delays, rise and fall times, Circuit design of inverters, complex gates with given constraints.Circuit Simulation and Performance Estimation using SPICE.Layouts of Inverters & Complex gates, Layout Optimization, Design Rule Check (DRC), Electrical Rule Check (ERC), Comparison of Layout Vs. Schematics, Circuit Extraction.
A project based on the above exercises.
Analog IC Design: Introduction to Analog Design tools, Review of EDA Tools. Analysis of Various Analog Building Blocks such as, Current and Voltage,References/Sources, Current Mirrors, Differential Amplifier, Output Stages design and analysis of Op-Amp and its Characterization. Analog Layout Constraints, Layout Designs and Analysis.

TESTING AND VERIFICATION OF VLSI DESIGN LAB Intoduction to Testing and Verification tools & Language like SystemC, Vericity - specman Elite, sure cov, Bus functional model (BFM), Test Bench generation using HDL based simulators, PLI / FLI , TCL / Tk

SEMINAR /CASE STUDY :
A student is required to select advance topic relevant to subject studies. The student should refer and review literature from IEEE and equivalent journals/proceedings, prepare and present report based on this.Each student will be assign at least one case study for each will make a presentation and submit a report based on this

SEMESTER III

HARDWARE-SOFTWARE CO-DESIGN :
Models of computation for embedded systems, Behavioral design, Architecture selection, Partitioning, scheduling, and communication, Simulation, synthesis, and verification, Hardware/software implementation, Performance analysis and optimization, Design methodologies and tools, Design examples and case studies

ASIC DESIGN LAB : VHDL Modeling and Simulation: Introduction to High Level Design Tools : Introduction & Familiarity with High Level Design Tools from various vendors e.g. Cadence, MentorTools, Sypnosis, ModelSim etc. Design & Simulation: Modeling and Simulation of systems/subsystems using HDLs e.g. VHDL / Verilog.
CAD for VLSI: Various CAD Tools for front end and Back end ASIC design,Schematic editors, Layout editors, Module generators, Place and Route tools, Floor planning, Behavioral, functional, logic and circuit simulators, Aids for test generation and testing , High-level synthesis tools
Project Work: A project based on the above exercise

MINI PROJECT (ELECTIVE)
Project based on VLSI Communication and signal processing end to end solution

MAJOR PROJECT: PART - I :A student is required to carry out elaborated project work. The project may be either design and fabrication work or a simulation and synthesis of a problem/system, develop algorithms and verify the feasibility on a computer. At the end of the semester student will be required to submit a detailed report of literature survey, design problem formulation,analysis, functional simulation and synthesis, work plan and work done and will defend his/her work carried out before examiners.

SEMESTER IV

MAJOR PROJECT: PART II :
A student will continue to work such as checking and testing synthesized system, layout, placement and routing the system, refine design to meet specifications, download design to FPGA/CPLD/ASIC or extract parasitics etc. on the project undertaken during semester III and at the end of the semester he/she will submit a thesis as a partial fulfillment of the M. Tech. Degree and defend his/her work before examiners.